Replacement Sheet

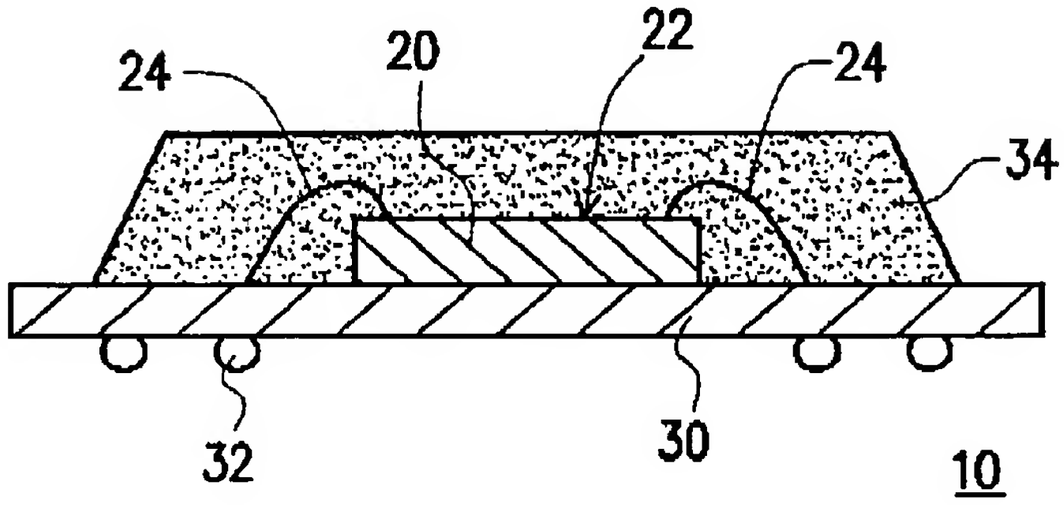

FIG. 1 (PRIOR ART)

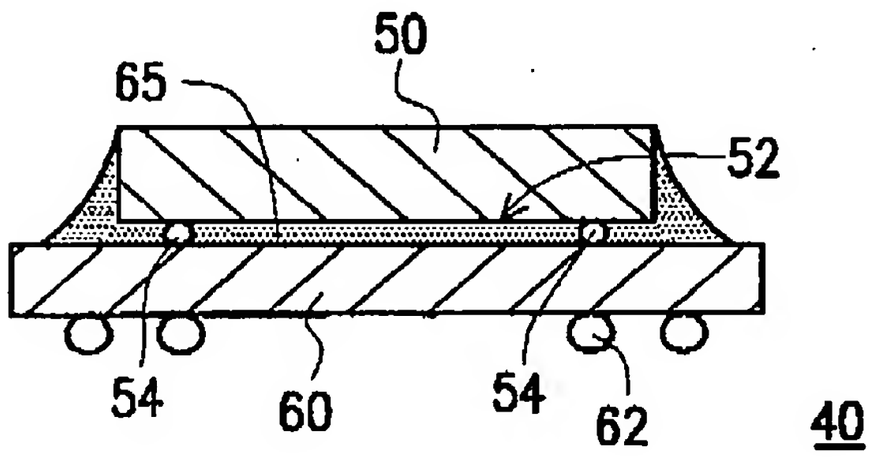

FIG. 2 (PRIOR ART)

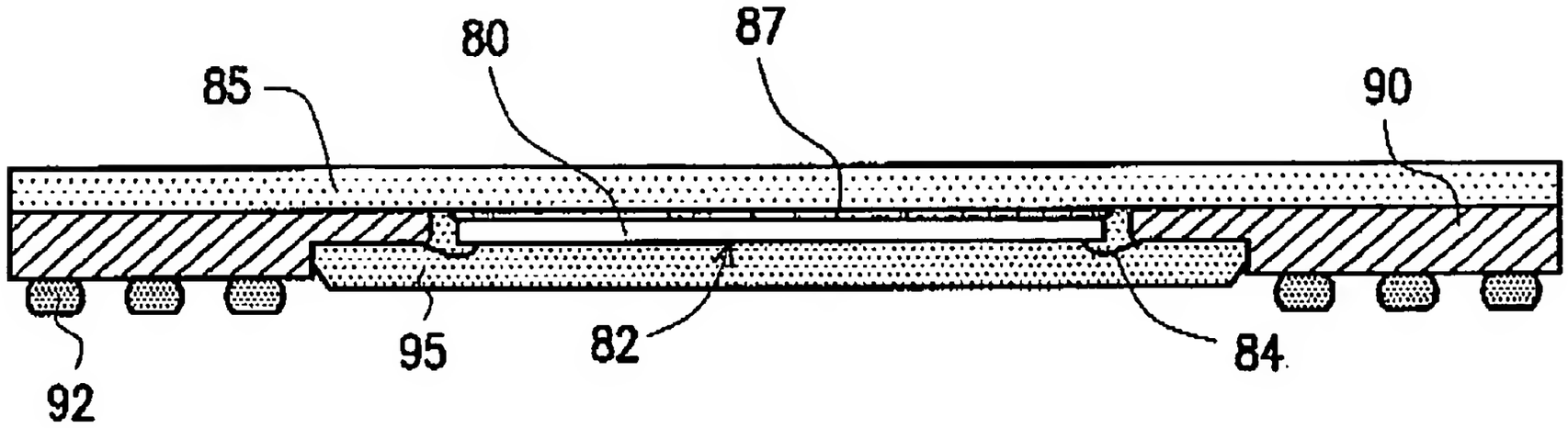

FIG. 3 (PRIOR ART)

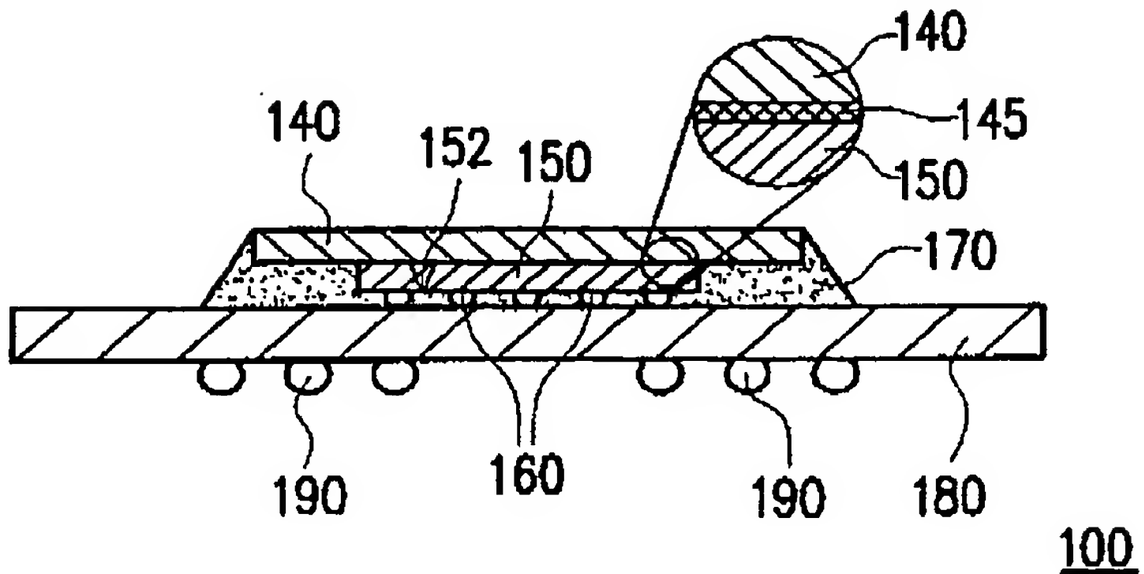

FIG. 4A

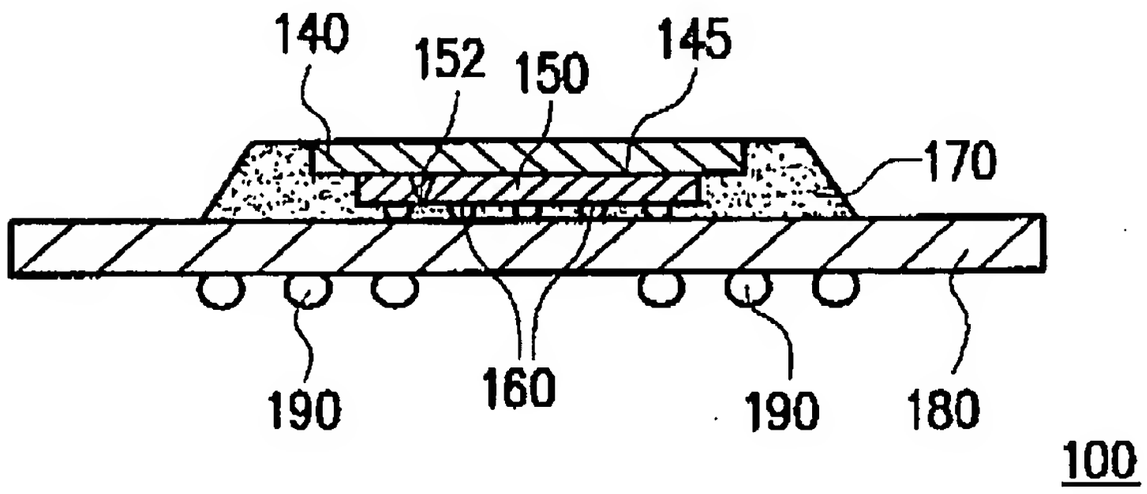

FIG. 4B

FIG. 4C

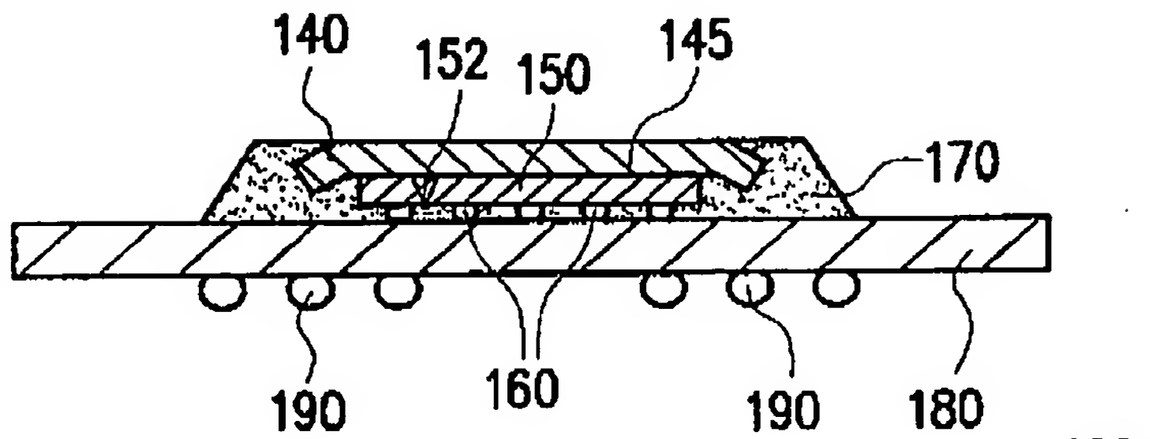

FIG. 4D

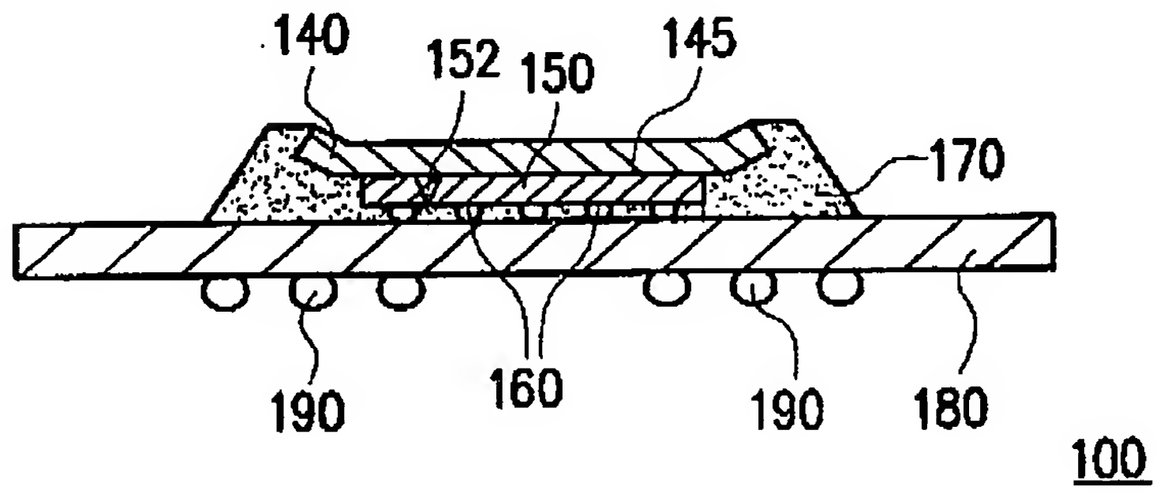

FIG. 4E

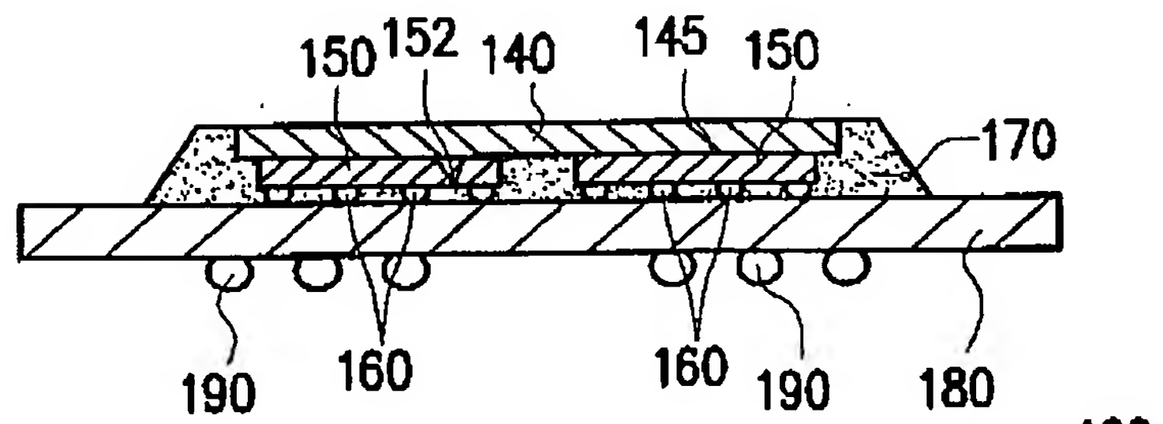

FIG. 4F

Replacement Sheet

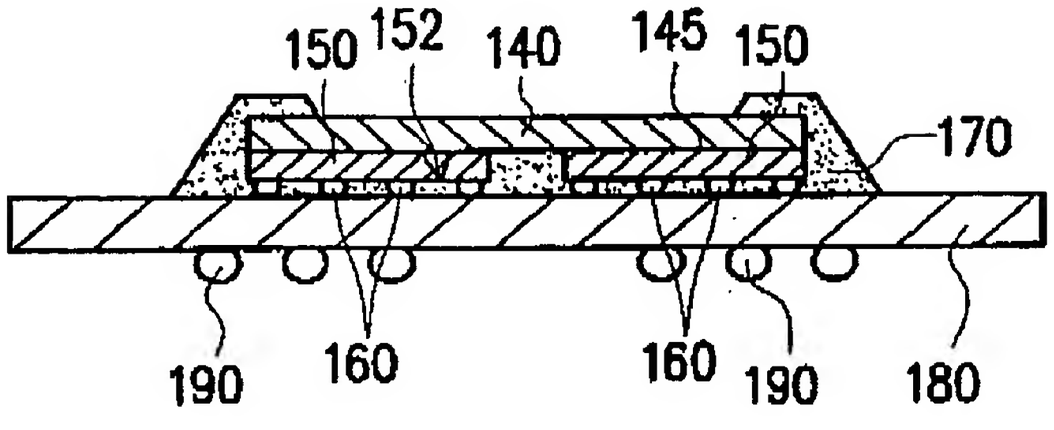

FIG. 4G

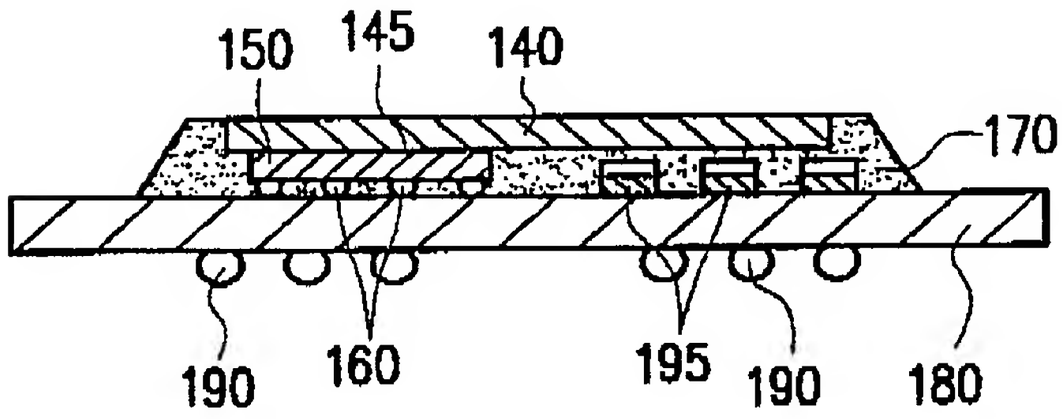

FIG. 4H

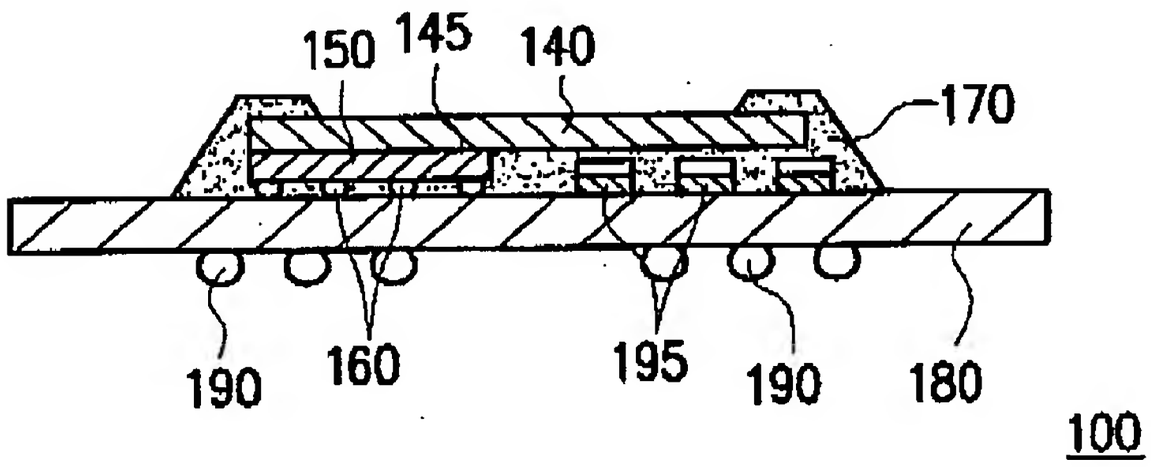

FIG. 14I

Replacement Sheet

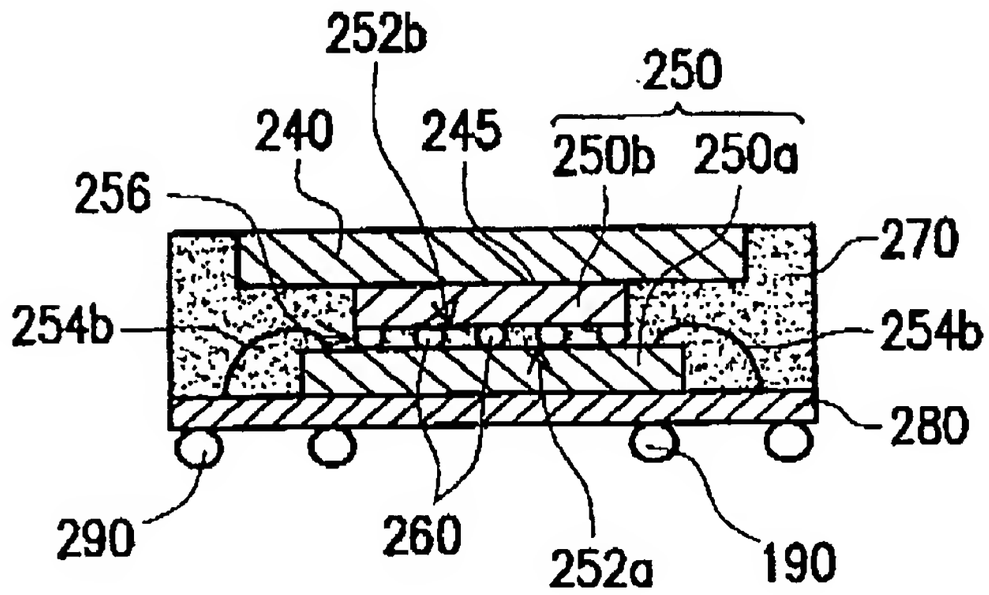

FIG. 5

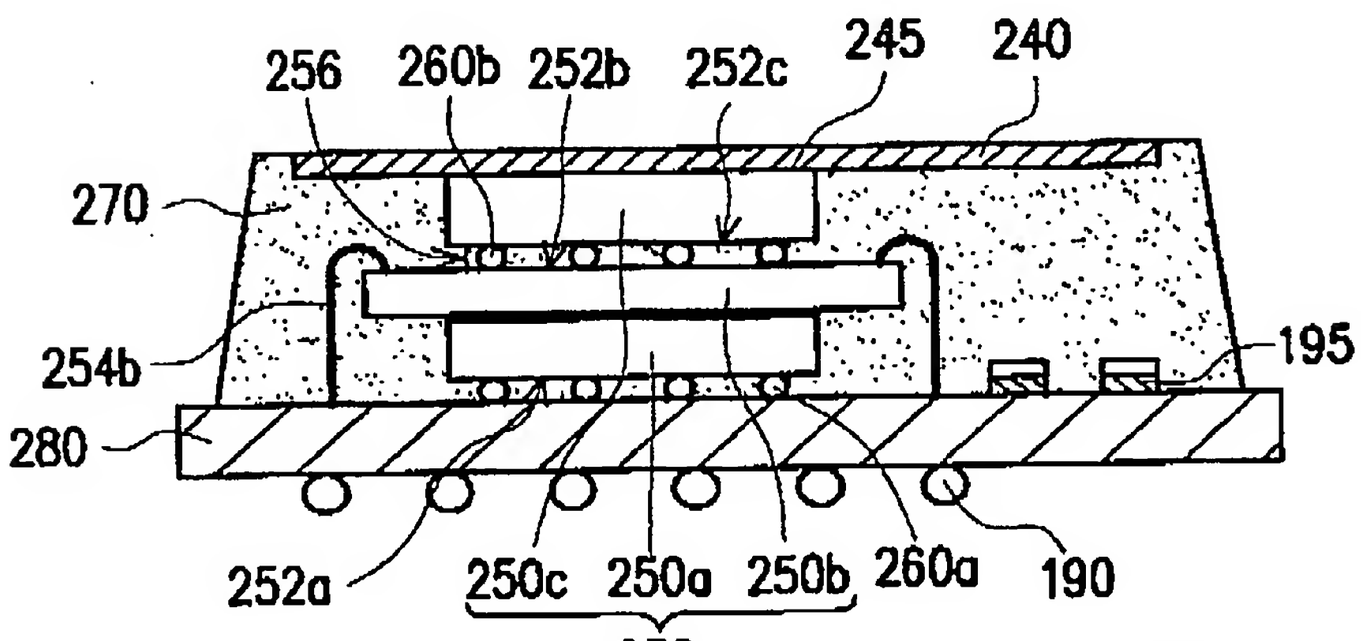

FIG. 6

Replacement Sheet

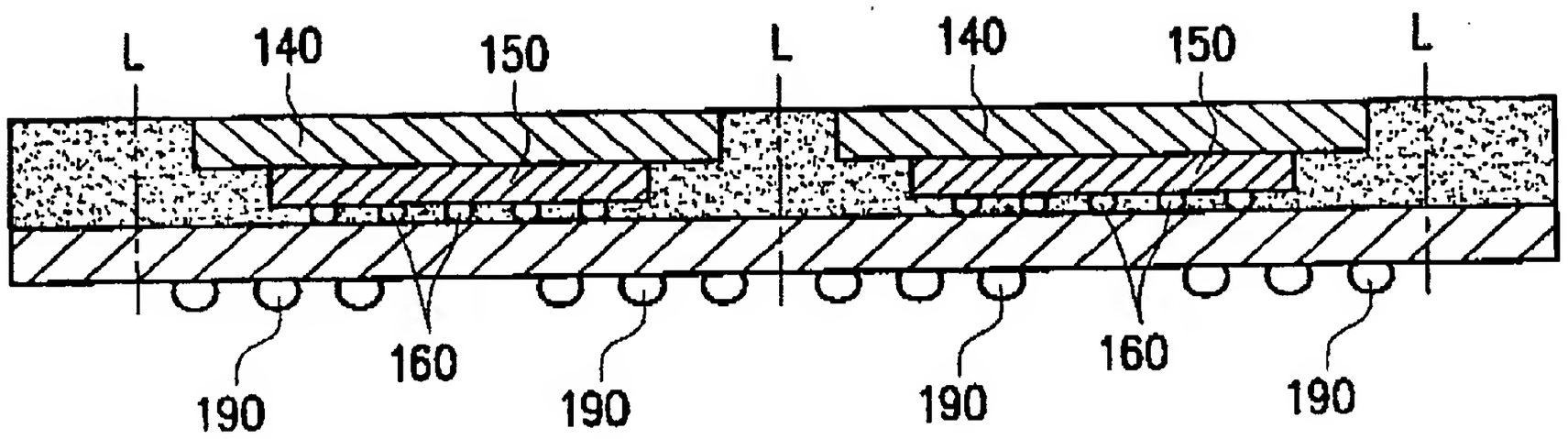

FIG. 7A

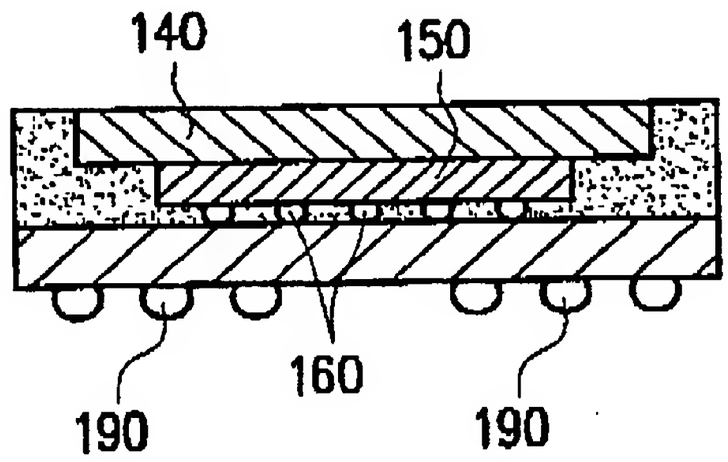

FIG. 7B

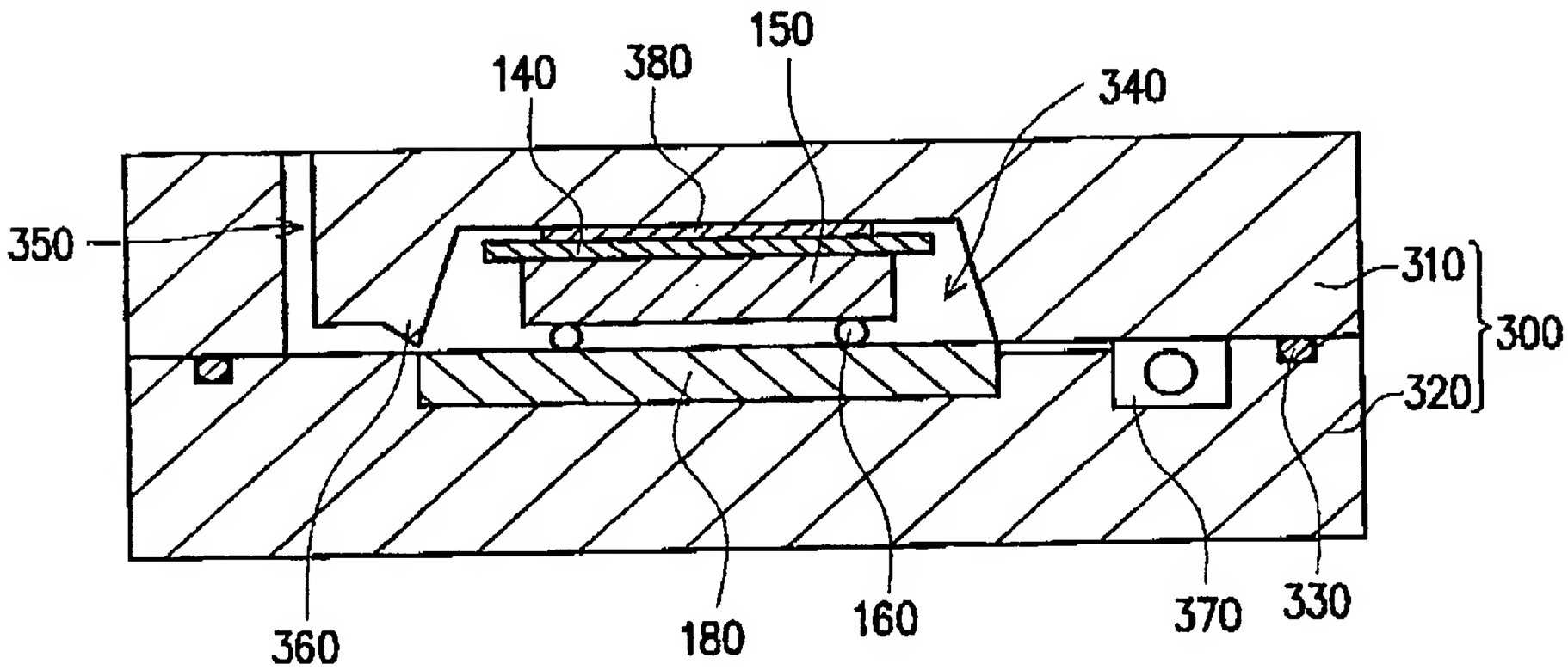

FIG. 8

	Example 1	Contrast example 1	Contrast example 2	Example 2	Example 3	Example 4	Example 5
Metallic surface flush	OK	OK	OK	OK	OK	OK	OK
Flip-chip bonding gap filling capacity *2	100%	100%	15%	99%	97%	100%	100%
Solder persistence *3	▲	O	X	O	O	▲	▲
Temperature recycle reliability *4	2000 cycles	500 cycles	--	2000 cycles	2000 cycles	2000 cycles	2000 cycles
PCT Reliability *5	>500 hours	168 hours	--	>500 hours	>500hour	>500 hours	>500 hours
Others							@

	Contrast example 3	Contrast example 4	Example 6	Example 7	Example 8	Contrast example 5	Contrast example 6
Metallic surface flush	OK	OK	OK	OK	OK	Maximum 2mm	OK
Flip-chip bonding gap filling capacity *2	40%	30%	100%	100%	100%	100%	100%
Solder persistence *3	X	X	▲	▲	▲	▲	▲
Temperature recycle reliability *4	--	--	2000 cycles	2000 cycles	2000 cycles	2000 cycles	--
PCT Reliability *5	--	--	>500 hours	>500 hours	>500 hours	>500 hours	--
Others							

*2 relative to chip area, material filling area ratio (filling capacity) average value using SAT criteria

*3 solder persistence: ▲: JEDEC level II passed; O: JEDEC level III passed; (n = 11) X: JEDEC level III failed

*4 temperature recycle reliability: gaseous surrounding, 65°C/15min ~ 150°C/15min (n = 11)

*5 PCT reliability 121°C/2atms

@ assessed using a total of 32 molded devices, 2 defective devices/remaining non-defective devices

Fig. 10